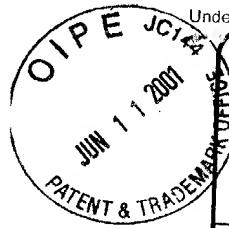


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## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Sheet 1 of 1

Substitute for form 1449A/PTO				Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	09/751,526
				Filing Date	12-29-00
				First Named Inventor	Nandu J. Marketkar, et al.
				Group Art Unit	2631
				Examiner Name	Not yet assigned
				Attorney Docket Number	42390.P10081
Sheet	1	of	2		

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Examiner Signature	<i>Rose H. Neal</i>	Date Considered	3/22/03
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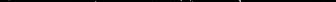
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Substitute for form 1449B/PTO		Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		Application Number	09/751,526
(use as many sheets as necessary)		Filing Date	12-29-00
		First Named Inventor	Nandu J. Marketkar, et al.
		Group Art Unit	2631
		Examiner Name	Not yet assigned
Sheet	2	of	2
		Attorney Docket Number	42390.P10081

#### OTHER PRIOR ART – NON-PATENT LITERATURE DOCUMENTS

Examiner Signature		Date Considered	3/21/03
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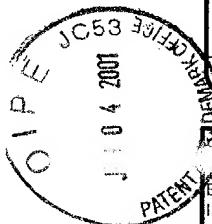
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of

**Complete if Known**

Application Number	09/751,526
Filing Date	12-29-00
First Named Inventor	Marketkar, et al.
Group Art Unit	2631
Examiner Name	Not yet assigned



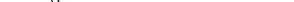
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

### Complete if Known

Application Number	09/751,526
Filing Date	12-29-00
First Named Inventor	Marketkar, et al.
Group Art Unit	2631
Examiner Name	Not yet assigned
Attorney Docket Number	42390P10081

### OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
JHA		Farjad-Rad, Ramin, et al., "A 0.3-μm CMOS 8-Gb/s 4-PAM Serial Link Transceiver", IEEE Journal of Solid-State Circuits, Vol. 35, No. 5, pp. 757-764 (May 2000).	
JHA		Osaka, Hideki, High Performance Memory Interface for DDR-SDRAM II: XTL (Crosstalk Transfer Logic), Hitachi Ltd., Systems Development Laboratory, pp. 1-20 (September 15, 2000).	
JHA		Stearns, Thomas H., Flexible Printed Circuitry, McGraw-Hill Companies, Inc., pp. 109-110 and 232-235 (1996).	
JHA		XTL Evaluation System, Hitachi Ltd., Systems Development Laboratory, pp. 1-14 (September 15, 2000).	
JHA		Yang, Chih-Kong Ken, et al., "A 0.5-μm CMOS 4.0-Gbit/s Serial Link Transceiver with Data Recovery Using Oversampling", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, pp. 713-722 (May 1998).	
JHA		U.S. Patent Application No. 09/713,702, filed November 15, 2000, entitled INTERCONNECT MECHANICS FOR ELECTROMAGNETIC COUPLER, by Nandu J. Marketkar, Thomas F. Knight, Jr., John R. Benham, Mark E. Naylor and John L. Critchlow.	
JHA		U.S. Patent Application No. 09/751,442, filed December 29, 2000, entitled CLAMP TO SECURE CARRIER TO DEVICE FOR ELECTROMAGNETIC COUPLER, by Nandu J. Marketkar, Mark E. Naylor and John L. Critchlow.	
JHA		U.S. Patent Application No. 09/751,527, filed December 29, 2000, entitled ELECTROMAGNETIC COUPLER SOCKET, by Nandu J. Marketkar, Thomas F. Knight, Jr., Mark E. Naylor and John L. Critchlow.	

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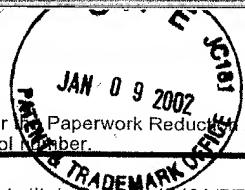
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Sheet 1 of 1

<i><b>Complete if Known</b></i>	
<b>Application Number</b>	09/751,526
<b>Filing Date</b>	12-29-2000
<b>First Named Inventor</b>	Marketkar, et al.
<b>Art Unit</b>	2631
<b>Examiner Name</b>	Not yet assigned
<b>Attorney Docket Number</b>	42390.P10081

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Sheet 1 of 1

<i><b>Complete if Known</b></i>	
<b>Application Number</b>	09/751,526
<b>Filing Date</b>	December 29, 2000
<b>First Named Inventor</b>	Marketkar, et al.
<b>Art Unit</b>	2631
<b>Examiner Name</b>	Not yet assigned
<b>Attorney Docket Number</b>	42390P10081

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Sheet 1 of 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				<i>Complete if Known</i>	
Sheet	1	of	1	Application Number	09/751,526
				Filing Date	12-29-2000
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				Examiner Name	Not assigned
				Attorney Docket Number	42390P10081

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